ABSTRACT

A PLL/DLL circuit is current self-biased responsive to a current I_{ld} provided from a voltage regulator to a VCO or VCDL. Bias current I_{bias}, which is proportional to I_{ld}, is provided to components of the PLL/DLL, such as a charge pump or loop resistor, from an interconnect coupled to the voltage regulator. In an embodiment of the present invention, a component of the PLL/DLL includes a bias-generating device, such as a MOSFET p-type transistor having a drain coupled to the interconnect. In an embodiment of the present invention, a voltage regulator includes an AMP having a bias-generating device, such as a p-type transistor, acting as a current source, having a source coupled to V_{dd} and a drain coupled to the interconnect. The gate of the bias-generating device is coupled to the gate of four other p-type devices. Each of the four p-type devices has a source coupled to V_{dd}. The drains of the first and second p-type transistors are coupled to an output providing I_{ld}. A negative input of the AMP ("INM") is coupled to the gate of a first n-type transistor and a positive input of the AMP ("INP") is coupled to the gate of a second n-type transistor. The drains of the first and second n-type transistors are coupled to the drains of the second and third p-type transistors. The sources of the first and second n-type transistors are coupled to the drain of a third n-type transistor. The source of the third n-type transistor is coupled to ground and the gate is coupled to a fourth n-type transistor. The drain of the fourth n-type transistor is coupled to the drain of the fourth p-type transistor and the source of the fourth n-type transistor is coupled to ground.